ALPHA DATA

# FMC-IPASS
# User Manual

**Revision: V1.0**

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# 1 Introduction

The FMC-IPASS is a VITA 57.1 compliant Single Width HPC FMC module, designed for use with Alpha Data's VITA 57.1 compliant carrier cards. It provides the user with the connectivity to implement high-speed serial IO communication applications.

This adapter board provides the connection between the FPGA card and industry standard 8x iPASS connectors similar to those used with PCI Express Cabling.

Maximum total bandwidth = 192Gbps (12Gbps per channel per direction)

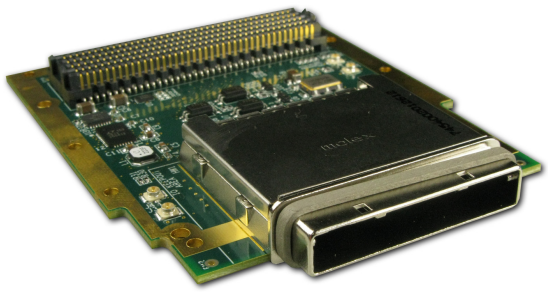

**Figure 1 : FMC-IPASS Image**

**Key Features**

- FMC (VITA 57.1) compliant
- Conduction and air cooled compatible
- 8 lanes of up to 12Gbps Serdes capable of PCIe gen3, 10GbE, and many other signaling standards
- Operating temperature range from -45 to 85 degrees Celsius
- Compatible with Samtec active optical cables
- Up to four serial channels and 4x 3.3V GPIO on Alpha Data FMC GPIO

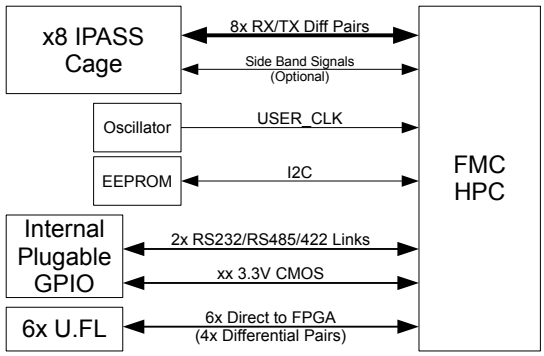


**Figure 2 : FMC-IPASS Block Diagram**

## 1.1 References & Specifications

| | |
|---|---|
| ANSI/VITA 57.1 | FPGA Mezzanine Card (FMC) Standard, February 2010, VITA, ISBN 1-885731-49-3 |

**Table 1 : References**

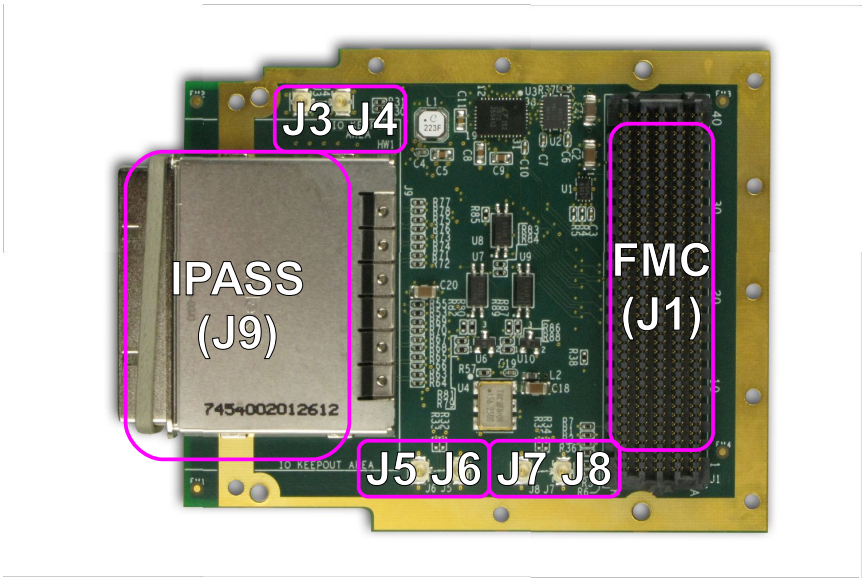


**Figure 3 : FMC-IPASS Top Side Features**

# 2 High Speed Serial IO (HSSIO)

## 2.1 Line Decoupling

The FMC Standard requires that the FMC module fit the appropriate AC coupling capacitors for the application. Because this board supports multiple signaling standards, there is not one solution. By default, the C2M (carrier to mezzanine) signals are AC coupled. However, there are 0 Ohm resistors on the M2C (mezzanine to carrier) signals that can be fitted with capacitors if needed.

## 2.2 User Clock

The user can specify a custom clock frequency that is directed to the FPGA banks associated with the high speed serial signals from this module. This enables support for a multitude of high speed serial IO communication protocols. The custom clock frequency is specified in the part number. See ordering information for more detail.

## 2.3 Connectors

The iPASS connector on the FMC-iPASS offers the user a wide selection of interconnect schemes that break out the multi-gigabit transceivers on the FPGA.

**Receptacle**

- iPASS connector system: Molex part numbers 75586-0007 and 74540-0201

## 2.4 Mating Cables

Below is a list of possible mating cables for the iPASS receptacle:

Optical cable termination available in LC, MPO, QSFP, and I-Pass

**Cable Solutions**

- For active optics running 10GbE or similar use Samtec OTP-173568-01-PCIEO
- For active optics running PCIe use Samtec PCIEO-8G2-005-005
- For copper cables use Molex 0745460801 or similar

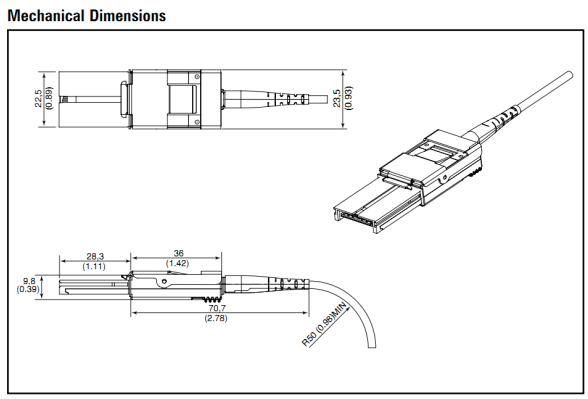


**Figure 4 : Samtec Active Optical Cable**

# 3 General Purpose IO

## 3.1 Overview

This FMC module provides the user access to a number of general purpose connectors that can be used for many different functions. The GPIO interface can be broken down into three components:

### 3.1.1 Direct Connections to the FPGA

There are three differential pairs accessible through industry standard U.FL connectors. These pairs are ideal for clocking and synchronization.

### 3.1.2 Serial Interface

The FMC hosts a Linear Technology LTC2872 configurable serial transceiver. This transceiver can be configured through strapping resistors to run in the following configurations:

**Serial Transceiver Configurations**

- 4 channels of RS232
- 2 channels of RS232 and 1 channel of RS422
- 2 channels of 422

The default mode of operation is: 2 channels of 422. Please see the LTC2872 datasheet for more details on configurability. All 11 configuration signals are tied to strapping resistors and can be configured to your specific needs by contacting sales@alpha-data.com.

### 3.1.3 General Purpose IO

Four signals from the FPGA are level translated to 3.3V and made available on the GPIO connector. The level translator is capable of driving both open-drain and push-pull signals.

## 3.2 Connectors

In order to guarantee the safety of the FPGA and enhance usability, this GPIO interface has been broken into multiple connectors.

**Receptacles**

- GPIO Connector: I-PEX part number 20455-020E-12
- UFL Connector: Hirose part number U.FL-R-SMT-1(10)

## 3.3 Mating Cables

Below is a list of possible mating cables for each associated receptacle.

**Receptacles**

- GPIO Connector: Alpha Data adapter pigtail part number AD-FMC-GPIO
- UFL Connector: Industry standard U.FL cable (multiple vendors)

# 4 Installation

The FMC-IPASS is designed to plug into the FMC front panel connector on a compatible carrier. The retaining screws should be tightened to secure the FMC.

**Note:**
This operation should not be performed while the host carrier is powered.

## 4.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions and avoid flexing the board.

## 4.2 IO Voltage Selection

The required IO voltage range (VADJ) for the FMC is 1.2V to 3.3V. This is stored in a ROM on the FMC, as per VITA 57.1 for automatic configuration of supplies. The carrier is responsible for detecting and setting the IO voltage accordingly.

# 5 Order Code

Product Code: FMC-IPASS (f)

Oscillator Frequency(f)

| Product Code | FMC-IPASS (f) |
|---|---|
| User Clock Frequency (f) | Blank = 156.25MHz<br>/125 = 125MHz<br>/### = ###MHz |

**Table 2 : Order Code**

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# Appendix A: iPass Pin Assignments

## Appendix A.1: PCIe Control Signals

| FMC Signal | FMC (J1) | Function | \| | Function | FMC (J1) | FMC Signal |
|---|---|---|---|---|---|---|
| LA00_CC_P | G6 | dPWRGD | \| | PERST | G7 | LA00_CC_N |
| LA01_CC_P | D8 | WAKE | \| | - | D9 | LA01_CC_N |

**Table 3 : PCIe Control Signal Locations**

## Appendix A.2: Clock Signals

| FMC Signal | FMC (J1) | Function | \| | Function | FMC (J1) | FMC Signal |
|---|---|---|---|---|---|---|
| GBTCLK0_M2C_P* | D4 | USER_CLK_P | \| | USER_CLK_N | D5 | GBTCLK0_M2C_N* |

**Table 4 : User Clock Location**

## Appendix A.3: High Speed Serial IO

| FMC Signal | FMC (J1) | Function | \| | Function | FMC (J1) | FMC Signal |
|---|---|---|---|---|---|---|
| DP0_M2C_P | C6 | PERp0 | \| | PETp0 | C2 | DP0_C2M_P |
| DP0_M2C_N | C7 | PERn0 | \| | PETn0 | C3 | DP0_C2M_N |
| DP1_M2C_P | A2 | PERp1 | \| | PETp1 | A22 | DP1_C2M_P |
| DP1_M2C_N | A3 | PERn1 | \| | PETn1 | A23 | DP1_C2M_N |
| DP2_M2C_P | A6 | PERp2 | \| | PETp2 | A26 | DP2_C2M_P |
| DP2_M2C_N | A7 | PERn2 | \| | PETn2 | A27 | DP2_C2M_N |
| DP3_M2C_P | A10 | PERp3 | \| | PETp3 | A30 | DP3_C2M_P |
| DP3_M2C_N | A11 | PERn3 | \| | PETn3 | A31 | DP3_C2M_N |
| DP4_M2C_P | A14 | PERp4 | \| | PETp4 | A34 | DP4_C2M_P |
| DP4_M2C_N | A15 | PERn4 | \| | PETn4 | A35 | DP4_C2M_N |
| DP5_M2C_P | A18 | PERp5 | \| | PETp5 | A38 | DP5_C2M_P |
| DP5_M2C_N | A19 | PERn5 | \| | PETn5 | A39 | DP5_C2M_N |
| DP6_M2C_P | B16 | PERp6 | \| | PETp6 | B36 | DP6_C2M_P |
| DP6_M2C_N | B17 | PERn6 | \| | PETn6 | B37 | DP6_C2M_N |
| DP7_M2C_P | B12 | PERp7 | \| | PETp7 | B32 | DP7_C2M_P |
| DP7_M2C_N | B13 | PERn7 | \| | PETn7 | B33 | DP7_C2M_N |

**Table 5 : Serial Channel Locations**

**Note:**
The function names match the PCI express cable standard

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# Appendix B: Alpha Data GPIO Pin Assignments

| FMC Signal | FMC (J1) | Function (Connector) | | Function (Connector) | FMC (J1) | FMC Signal |
|---|---|---|---|---|---|---|
| HB00_CC_P | K25 | UFL_0_P (J3) | \| | UFL_0_N (J4) | K26 | HB00CC__N |
| HB01_P | J24 | UFL_1_P (J5) | \| | UFL_1_N (J6) | J25 | HB01_N |
| HB02_P | F22 | UFL_2_P (J7) | \| | UFL_2_N (J8) | F23 | HB02_N |
| HB03_P | E21 | DY1 (Serial TX) | \| | RA1 (Serial RX) | E22 | HB03_N |
| HB04_P | F25 | DY2 (Serial TX) | \| | RA2 (Serial RX) | F26 | HB04_N |
| HB05_P | E24 | GPIO_0 | \| | GPIO_1 | E25 | HB05_N |
| HB06_CC_P | K28 | - | \| | - | K29 | HB06_CC_N |
| HB07_P | J27 | GPIO_2 | \| | GPIO_3 | J28 | HB07_N |

**Table 6 : GPIO Locations**

# Revision History

| Date | Revision | Changed By | Nature of Change |
|---|---|---|---|
| 25 Oct 2013 | 1.0 | K. Roth | Initial Release |

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